Serial ATA Logo Working Group

Serial ATA Interoperability Program Revision 1.4

Agilent MOI for SATA RXTX Tests

Using Agilent E5071C ENA Network Analyzer Option TDR

1. TABLE OF CONTENTS

2. MODIFICATION RECORD

Revision	Comments	Issue Date
1.00	Changed version number	Jan 12, 2011
1.00RC	Changed version number Update Figure 4-3 and Figure 7-1 to 7-12	Nov 11, 2010
0.90	Added Acknowledgement	Sep 23, 2010
0.80	Initial Draft Release	Sep 10, 2010

3. ACKNOWLEDGEMENTS

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4. RESOURCE REQUIREMENTS

4.1. LIST OF REQUIRED RESOURCE

This section describes the hardware/software requirements and basic test setup used for all tests in this MOI.

Custom SATA test fixtures are required for performing the physical layer tests covered in this document. The purpose of this section is also to present a reference implementation of these test fixtures, to specify the basic test equipment used for performing the tests contained in this document, and to define the basic test setup which is used for all tests.

The list below summarizes the measurement equipment required for performing the tests contained in this document.

• 1-Agilent E5071C Network Analyzer with option TDR and one of the following options: 48x/4D5/4K5

• Electronic Calibration Module N4431B (for 48x) or N4433A (for 4D5/4K5)

• Four 3.5 mm cables and adapters of 20 GHz bandwidth or equivalent

• One set of SATA fixture (below are the recommended fixtures)

   ➢ Agilent SAS Drive X2 Primary Test Fixture Agilent P/N N5421-26401

   ➢ Crescent Heart Software P/N TF-SATA-NE-ZP/TF-SATA-FE-ZP

   ➢ ICT Solutions P/N TF-1R31/TF1P21

   ➢ Wilder Technologies P/N SATA-TPA-R 600-1014-000/600-1013-000

• 1 – Means for configuring SATA BIST modes (Ulink DriveMaster or SerialTek BusXpert, or equivalent.)

4.2.   FIXTURE IMPLEMENTATION

Figure 4-1: Agilent SAS/SATA Drive Test Fixture
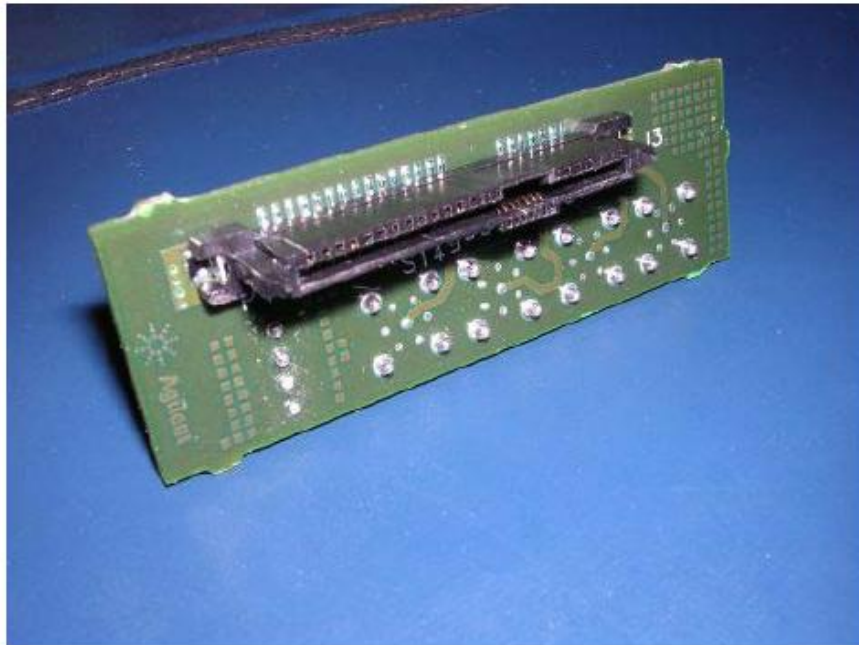
Figure 4-2: Agilent SAS/SATA Drive Test Fixture (Reverse)

Above is a picture of the Agilent SAS Primary X2 Drive Fixture, which converts a SAS/SATA connector to 4 SMAs in order to make signal quality measurements.

TEST SETUP

Shown below is the basic setup used for all tests in this MOI. Port 1 and 2 of the instrument are connected to TX and Port 3 and 4 to RX pair of the PUT(for tests TX-xx or RX-xx, respectively), while the PUT is powered using a standard PC power supply.
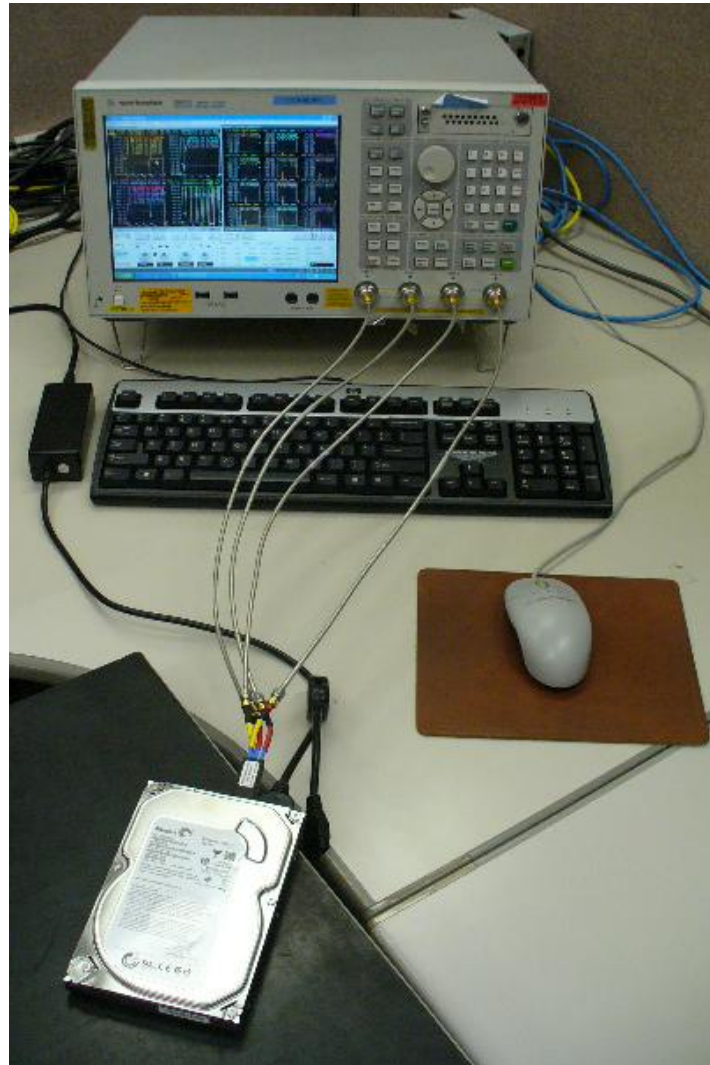
Figure 4-3: General Test Setup with E5071C Network Analyzer

5. MEASUREMENT SETUP

5.1. RECALLING STATE FILE

This section describes how to recall a state file for SATA TXRX compliance testing. Using the state file distributed on www.agilent.com/find/ena-tdr_sata-txrx, the setup operation can be skipped. Download the file that matches the E5071C option, and extract the file. If you use your local PC to download, save the state file to a USB mass storage device in order to move it to the E5071C. Connect the USB mass storage device into the USB port on the front panel of the E5071C. For manual measurement setup, refer to Chapter 7.1. TIME DOMAIN MEASUREMENT SETUP MANUALLY and Chapter 7.2. FREQUENCY DOMAIN MEASUREMENT SETUP MANUALLY.

*Note: Hard Keys (Keys located on the Front panel of E5071C) are displayed in Blue color and **Bold**. (Example: **Avg**, **Analysis**)*

*Note: Soft keys (Keys on the screen) are displayed in **Bold**. (Example: **S11**, **Real**, **Transform**)*

*Note: Buttons (in the TDR) are displayed in Green color and **Bold**. (Example: **Trace**, **Rise Time**)*

*Note: Tabs (in the TDR) are displayed in Brown color and **Bold**. (Example: **Setup**, **Trace Control**)*

1. If TDR setup wizard appears, click **Close** button on the TDR setup wizard.
2. Open **Setup** tab (item1).
3. Click **Advanced Mode** (item2).
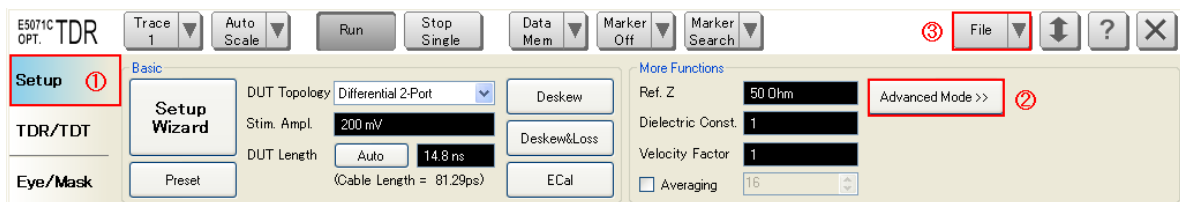
4. A dialog box appears requesting for confirmation. Then click **Yes**. (Clear the check box for "Use Advanced Calibration Methods")
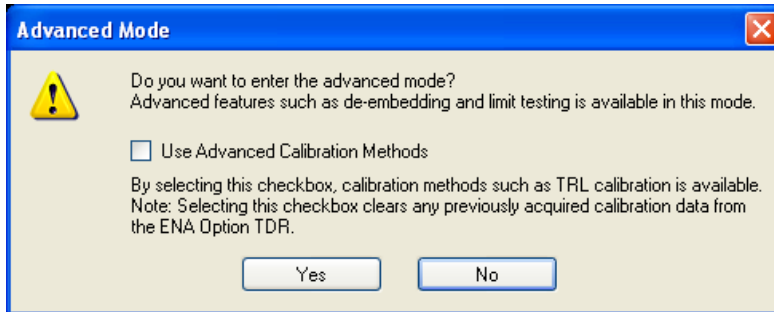
5.   Click **File** (item3) and select **Recall State** to open the Recall State dialog box.

6.   Specify a folder and a file name, and click **Open**.

5.2.   MEASUREMENT CONFIGURATION

The figure 5-1 describes the screen configuration of the E5071C.   Channel 1 for time domain measurement is controlled by the TDR user interface at the bottom of the screen, and Channel 2 for frequency domain measurement is controlled by the softkey on the right side of the screen or hardkey on the instrument front panel.   Measurement parameter for each window is described in Figure 5-2.
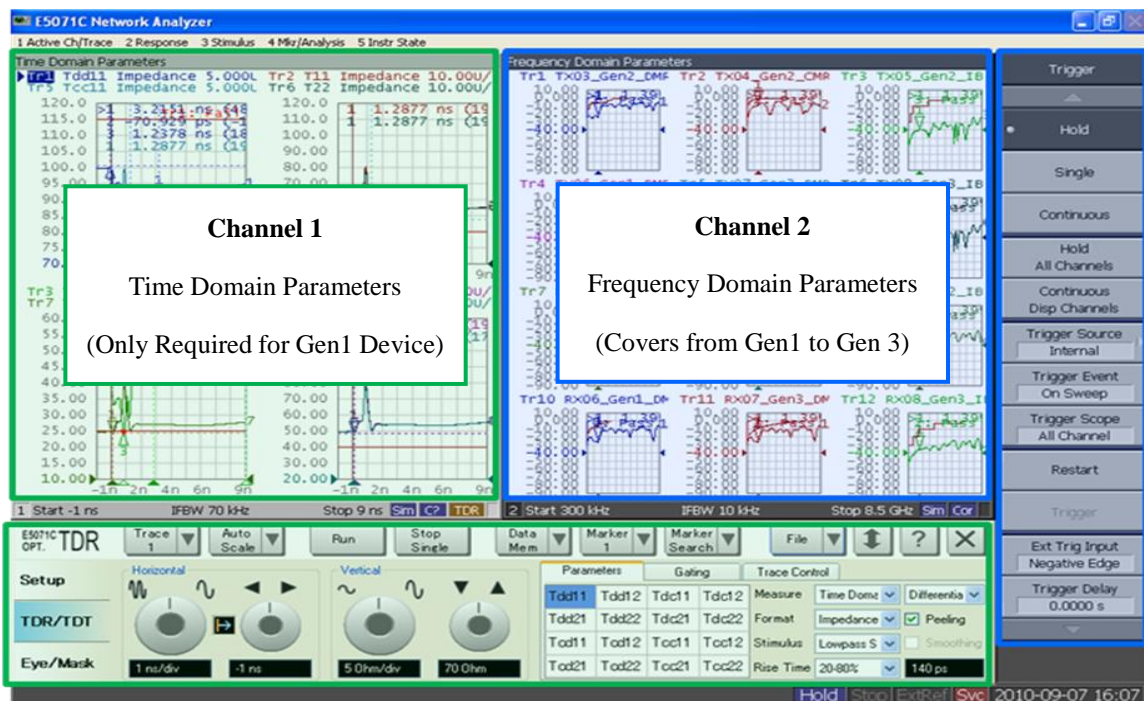
Figure 5-1 Description of Screen Configuration
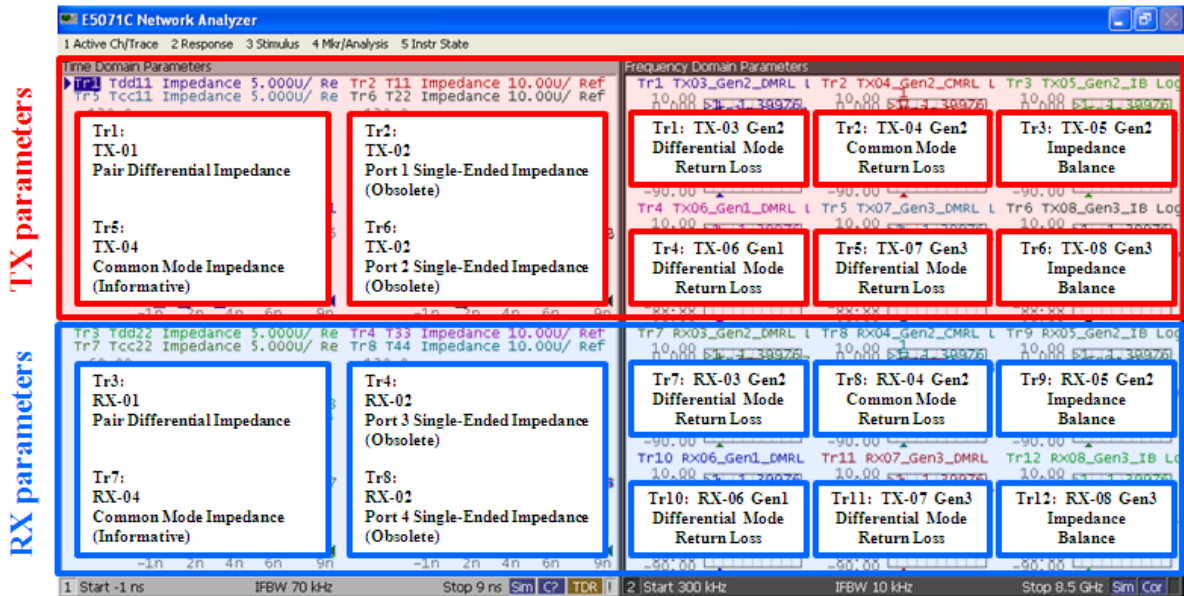
Figure 5-2 Description of Measurement Window

Note: Tr # stands for Trace #, Port # stands for the instrument port #.

5.3.   CALIBRATION

5.3.1.   Time Domain Calibration

1.   Press **Channel Next** key to select Channel1.

1.   Open **Setup** tab (item1).

2.   Click **ECal** (item2) to launch TDR Setup Wizard.
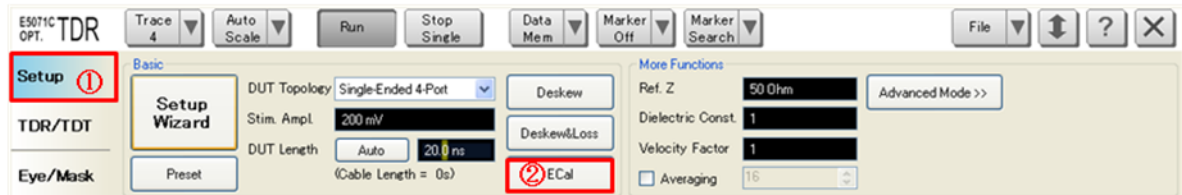
3.   Connect the test cables to the ECal module.

4.   Click **Calibrate** button, then click **Next >**.
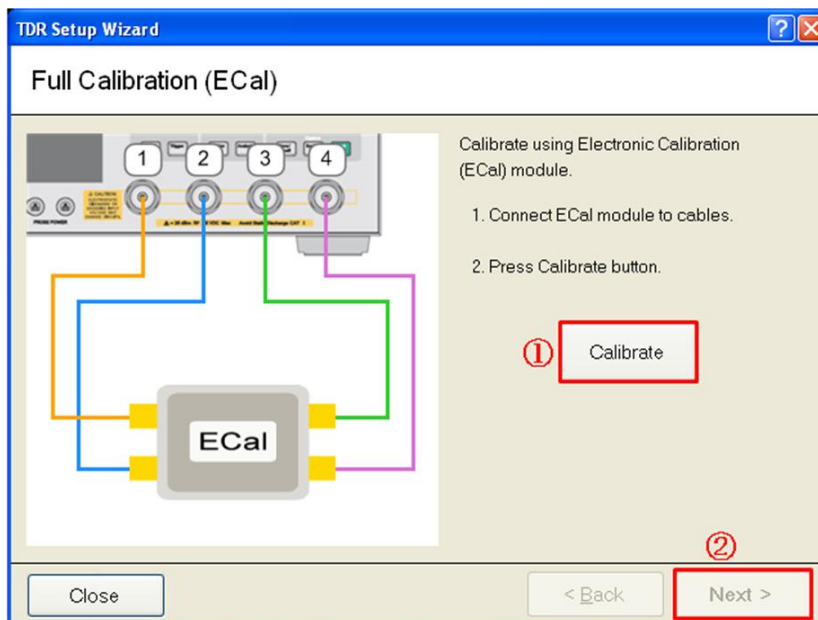
5.   Click **Finish** (item1).
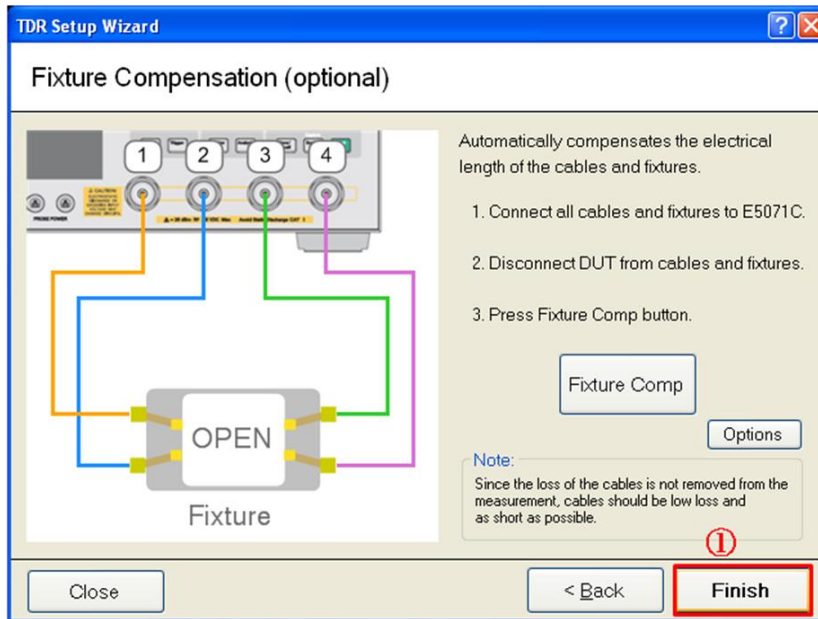
5.3.2. Frequency Domain Calibration

1. Press **Channel Next** key to select channel 2.

2. Press **Cal** > ECal > 4-Port Cal

5.3.3. Rise Time Adjustment

The system rise time is set as close to 100 psec as practical.

1. Press **Channel Next** key to select Channel1.

2. Press **Channel Max** key to enlarge Channel1.

3. Connect the calibrated SMA cables from port 1 and 2 of the E5071C to the TX+ and TX- connectors of the SATA-to-SMA Test Fixture.   Leave the test fixture at OPEN.

4. Select **Trace1**.

5. Open **TDR/TDT** tab.

6. Select **Volt** from **Format** menu.

7. Activate **Marker 5** from **Marker** menu.

8. Select **Rise Time (20-80%)** from **Marker Search** menu.

9. Click **Run** button.

10. Adjust **Rise Time** so that the marker value on Trace1 may be close to 100 psec, and note the input value.

11. Set Trace1 setting to the original by selecting **Impedance** from **Format** menu.   Then select **Marker 5** from **Marker** menu to deactivate marker 5.

12. Set the rise time to the noted value on the other traces in Channel1.

13. Press **Channel Max** key to get Channel1 back to the normal size.

6. MEASUREMENT AND DATA ANALYSIS

6.1. INTRODUCTION

The tests contained in this document are organized in order to simplify the identification of information related to a test, and to facilitate in the actual testing process.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. Formally, each test description contains the following sections:

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

This section specifies all reference material *external* to the MOI, including the specific subclauses references for the test in question, and any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by a bracketed number (e.g., [1]) when mentioned in the test description. Any other references in the test description that are not indicated in this manner refer to elements within the MOI document itself (e.g., "Appendix 7.1.", or "Figure 6.1")

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here as well.

Test Procedure

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

6.2. GROUP 1: PHY TRANSMITTER REQUIREMENTS

Overview:

This group of tests verifies the Phy Transmitter Requirements, as defined in Section 2.14 of the Serial ATA Interoperability Program Revision 1.4 Unified Test Document (which references the SATA Revision 3.0 standard)

6.2.1. TEST TX-01 - Pair Differential Impedance

Purpose: To verify that the Pair Differential Impedance of the PUT transmitter is within the conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.14.1

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 1.5Gb/s. For products that support a maximum operating speed of 3.0Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

Assuming the initial setup/cal procedures in chapter 5 have been performed, the measurement for this test is as follows:

1. Ensure that the PUT is powered on and is sourcing MFTP signaling at 1.5Gb/s.
2. Connect the SMA cables from port 1 and 2 of the E5071C to the TX+ and TX- connectors of the SATA-to-SMA Test Fixture.
3. Select Channel 1 and double click on Trace 1 to enlarge the window.   For Channel and Trace allocation, refer to chapter 5.2.
4. Adjust the scope timebase and delay to display the Pair Differential Impedance on the screen.
5. Using marker #3, determine the time point of the last major capacitive dip.   Perform averaging if necessary (Normally, 10 to 16 averaging times are adequate.)
6. Record the impedance value at the point occurring 2ns after the last major capacitive dip with marker #4 (See Figure 6-1, next page, for sample measurement.)
7. Also, record the overall maximum and minimum impedance values over the entire observation window with marker #1 and #2.
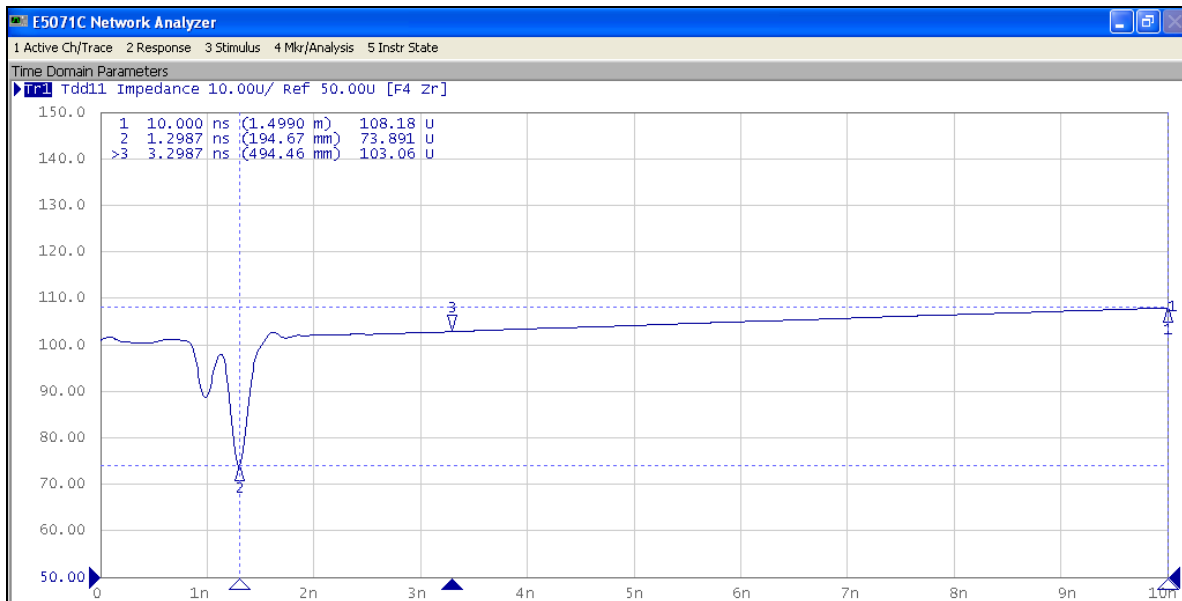
Figure 6-1: Sample Impedance Measurement at time point 2ns after last major dip

Observable Results:

All measured impedance values shall be between 85 and 115 ohms.

NOTE: The verification of this result may not be required. If a product which supports 1.5Gb/s passes TX-06, then it is not required that this result be verified (though the test should still be performed.)   This result must be verified for a 1.5Gb/s product if it fails TX-06.

NOTE: The 2ns measurement result is considered informative for this test.   Conformance is based on the overall impedance profile.

6.2.2.   TEST TX-02 - Single-ended Impedance (Obsolete)

Purpose: To verify that the Single-Ended Impedance of the PUT transmitter is within the conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.14.2

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 1.5Gb/s.   For products that support a maximum operating speed of 3.0Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

Assuming the initial setup/cal procedures in chapter 5 have been performed, the measurement for this test is as follows:

1. Ensure that the PUT is powered on and is sourcing MFTP signaling at 1.5Gb/s.
2. Connect the SMA cables from port 1 and 2 of the E5071C to the TX+ and TX- connectors of the SATA-to-SMA Test Fixture.
3. Select Channel 1 and double click on Trace 2 to enlarge the window.   For Channel and Trace allocation, refer to chapter 5.2.
4. Adjust the scope timebase and delay to display the Single-ended Impedance on the screen.
5. Record the minimum values of the Pair Single-Ended Impedance with marker #1.   Perform averaging if necessary (Normally, 10 to 16 averaging times are adequate.)
6. Repeat the above step 3 to 5 with Trace 6.

Observable Results:

For both responses, the measured impedance values shall be greater than 40 ohms.

6.2.3. TEST TX-03 - Gen2(3Gb/s) Differential Mode Return Loss

Purpose: To verify that the Differential Mode Return Loss of the PUT transmitter is within the conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.14.3

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 3.0Gb/s. For products that support a maximum operating speed of 1.5Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

Assuming the initial setup/cal procedures in chapter 5 have been performed, the measurement for this test is as follows:

1. Ensure that the PUT is powered on and is sourcing MFTP signaling at 3Gb/s.
2. Connect the SMA cables from port 1 and 2 of the E5071C to the TX+ and TX- connectors of the SATA-to-SMA Test Fixture.
3. Select Channel 2 and double click on Trace 1 "TX03_GEN2_DMRL". For Channel and Trace allocation, refer to chapter 5.2. Perform averaging if necessary (Normally, 10 to 16 averaging times are adequate.)

Observable Results:

The TX Differential Mode Return Loss shall be greater than the minimum limits specified in reference [1] for 3.0G products. For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (3.0G)
150-300 MHz	14 dB
300-600 MHz	8 dB
600-1200 MHz	6 dB
1200-2400 MHz	6 dB
2400-3000 MHz	3 dB (N/A for Gen1m)
3000-5000 MHz	1 dB (N/A for Gen1m/2m)

6.2.4.   TEST TX-04 - Gen2(3Gb/s) Common Mode Return Loss

Purpose: To verify that the Common Mode Return Loss of the PUT transmitter is within the conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.14.4

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 3.0Gb/s.   For products that support a maximum operating speed of 1.5Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

Assuming the initial setup/cal procedures in chapter 5 have been performed, the measurement for this test is as follows:

1. Ensure that the PUT is powered on and is sourcing MFTP signaling at 3Gb/s.
2. Connect the SMA cables from port 1 and 2 of the E5071C to the TX+ and TX- connectors of the SATA-to-SMA Test Fixture.
3. Select Channel 2 and double click on Trace 2 "TX04_GEN2_CMRL".   For Channel and Trace allocation, refer to chapter 5.2.   Perform averaging if necessary (Normally, 10 to 16 averaging times are adequate.)

Observable Results:

The TX Common Mode Return Loss shall be greater than the minimum limits specified in reference [1] for 3.0G products.   For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (3.0G)
150-300 MHz	8 dB
300-600 MHz	5 dB
600-1200 MHz	2 dB
1200-2400 MHz	1 dB
2400-3000 MHz	1 dB
3000-5000 MHz	1 dB

6.2.5. TEST TX-05 - Gen2(3Gb/s) Impedance Imbalance

Purpose: To verify that the Impedance Balance of the PUT transmitter is within the conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.14.5

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 3.0Gb/s. For products that support a maximum operating speed of 1.5Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

Assuming the initial setup/cal procedures in chapter 5 have been performed, the measurement for this test is as follows:

1. Ensure that the PUT is powered on and is sourcing MFTP signaling at 3Gb/s.
2. Connect the SMA cables from port 1 and 2 of the E5071C to the TX+ and TX- connectors of the SATA-to-SMA Test Fixture.
3. Select Channel 2 and double click on Trace 3 "TX05_GEN2_IB". For Channel and Trace allocation, refer to chapter 5.2. Perform averaging if necessary (Normally, 10 to 16 averaging times are adequate.)

Observable Results:

The TX Impedance Balance shall be greater than the minimum limits specified in reference [1] for 3.0G products. For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (3.0G)
150-300 MHz	30 dB
300-600 MHz	20 dB
600-1200 MHz	10 dB
1200-2400 MHz	10 dB
2400-3000 MHz	4 dB
3000-5000 MHz	4 dB (N/A for Gen2m)

6.2.6. TEST TX-06 - Gen1(1.5Gb/s) Differential Mode Return Loss

Purpose: To verify that the Differential Mode Return Loss of the PUT transmitter is within the Gen1 conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.14.6

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 1.5Gb/s.   For products that support a maximum operating speed of 3.0Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

Assuming the initial setup/cal procedures in chapter 5 have been performed, the measurement for this test is as follows:

1. Ensure that the PUT is powered on and is sourcing MFTP signaling at 1.5Gb/s.
2. Connect the SMA cables from port 1 and 2 of the E5071C to the TX+ and TX- connectors of the SATA-to-SMA Test Fixture.
3. Select Channel 2 and double click on Trace 4 "TX06_GEN1_DMRL".   For Channel and Trace allocation, refer to chapter 5.2.   Perform averaging if necessary (Normally, 10 to 16 averaging times are adequate.)

Observable Results:

The TX Differential Mode Return Loss shall be greater than the minimum limits specified in reference [1] for 1.5G products.   For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (1.5G)
75-150 MHz	14 dB
150-300 MHz	8 dB
300-600 MHz	6 dB
600-1200 MHz	6 dB
1200-2400 MHz	3 dB (N/A for Gen1m)
2400-3000 MHz	1 dB (N/A for Gen1m/2m)

6.2.7.   TEST TX-07 - Gen3(6Gb/s) Differential Mode Return Loss

Purpose: To verify that the Differential Mode Return Loss of the PUT transmitter is within the Gen3 conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.14.7

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 6.0Gb/s.   For products that support a maximum operating speed of 1.5Gb/s or 3.0Gb/s this test is not required.

Test Procedure:

Assuming the initial setup/cal procedures in chapter 5 have been performed, the measurement for this test is as follows:

1. Ensure that the PUT is powered on and is sourcing MFTP signaling at 6.0Gb/s.
2. Connect the SMA cables from port 1 and 2 of the E5071C to the TX+ and TX- connectors of the SATA-to-SMA Test Fixture.
3. Select Channel 2 and double click on Trace 5 "TX07_GEN3_DMRL".   For Channel and Trace allocation, refer to chapter 5.2.   Perform averaging if necessary (Normally, 10 to 16 averaging times are adequate.)

Observable Results:

The TX Differential Mode Return Loss shall be greater than the minimum limits specified in reference [1] for 6.0G products.   For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (6.0G)
300-3000 MHz	$14 - 13*log10(f/300E6)$ dB

6.2.8. TEST TX-08 - Gen3(6Gb/s) Impedance Imbalance

Purpose: To verify that the Impedance Imbalance of the PUT transmitter is within the Gen3 conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.14.8

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 6.0Gb/s. For products that support a maximum operating speed of 1.5Gb/s or 3.0Gb/s this test is not required.

Test Procedure:

Assuming the initial setup/cal procedures in chapter 5 have been performed, the measurement for this test is as follows:

1. Ensure that the PUT is powered on and is sourcing MFTP signaling at 6.0Gb/s.
2. Connect the SMA cables from port 1 and 2 of the E5071C to the TX+ and TX- connectors of the SATA-to-SMA Test Fixture.
3. Select Channel 2 and double click on Trace 6 "TX08_GEN3_IB". For Channel and Trace allocation, refer to chapter 5.2. Perform averaging if necessary (Normally, 10 to 16 averaging times are adequate.)

Observable Results:

The TX impedance Balance shall be greater than the minimum limits specified in reference [1] for 6.0G products. For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (6.0G)
150-300 MHz	30 dB
300-600 MHz	30 dB
600-1200 MHz	20 dB
1200-2400 MHz	10 dB
2400-3000 MHz	10 dB
3000-5000 MHz	4 dB
5000-6500 MHz	4 dB

6.3. GROUP 1: PHY RECEIVER REQUIREMENTS

Overview:

This group of tests verifies the Phy Receiver Requirements, as defined in Section 2.16 of the Serial ATA Interoperability Program Revision 1.4 Unified Test Document (which references the SATA Revision 3.0 standard)

6.3.1. TEST RX-01 - Pair Differential Impedance

Purpose: To verify that the Pair Differential Impedance of the PUT receiver is within the conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.16.1

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 1.5Gb/s. For products that support a maximum operating speed of 3.0Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

The procedure for this test is identical to that of test TX-01, with the exception of below two.

1. The SMA cables from port 3 and 4 of the E5071C shall be connected to the RX+ and RX- connectors of the SATA-to-SMA Test Fixture.
2. Target measurement parameter is displayed in Channel 1, Trace 3. For Channel and Trace allocation, refer to chapter 5.2.

Observable Results:

All measured impedance values shall be between 85 and 115 ohms.

NOTE: The verification of this result may not be required. If a product which supports 1.5Gb/s passes TX-06, then it is not required that this result be verified (though the test should still be performed.) This result must be verified for a 1.5Gb/s product if it fails TX-06.

NOTE: The 2ns measurement result is considered informative for this test. Conformance is based on the overall impedance profile.

6.3.2.   TEST RX-02 - Single-ended Impedance (Obsolete)

Purpose: To verify that the Single-Ended Impedance of the PUT transmitter is within the conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.16.2

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 1.5Gb/s.   For products that support a maximum operating speed of 3.0Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

The procedure for this test is identical to that of test TX-02, with the exception of below two steps.

1. The SMA cables from port 3 and 4 of the E5071C shall be connected to the RX+ and RX- connectors of the SATA-to-SMA Test Fixture.
2. Target measurement parameters are displayed in Channel 1, Trace 4 and 8.   For Channel and Trace allocation, refer to chapter 5.2.

Observable Results:

For both responses, the measured impedance values shall be greater than 40 ohms.

6.3.3. TEST RX-03 - Gen2(3Gb/s) Differential Mode Return Loss

Purpose: To verify that the Differential Mode Return Loss of the PUT receiver is within the conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.16.3

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 3.0Gb/s. For products that support a maximum operating speed of 1.5Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

The procedure for this test is identical to that of test TX-03, with the exception that the SMA cables from port 3 and 4 of the E5071C shall be connected to the RX+ and RX- connectors of the SATA-to-SMA Test Fixture. The measurement parameter is displayed in Channel 2, Trace 7 "RX03_GEN2_DMRL". For Channel and Trace allocation, refer to chapter 5.2.

Observable Results:

The RX Differential Mode Return Loss shall be greater than the minimum limits specified in reference [1] for 3.0G products. For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (3.0G)
150-300 MHz	18 dB
300-600 MHz	14 dB
600-1200 MHz	10 dB
1200-2400 MHz	8 dB
2400-3000 MHz	3 dB
3000-5000 MHz	1 dB

6.3.4. TEST RX-04 - Gen2(3Gb/s) Common Mode Return Loss

Purpose: To verify that the Common Mode Return Loss of the PUT receiver is within the conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.16.4

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 3.0Gb/s. For products that support a maximum operating speed of 1.5Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

The procedure for this test is identical to that of test TX-04, with the exception that the SMA cables from port 3 and 4 of the E5071C shall be connected to the RX+ and RX- connectors of the SATA-to-SMA Test Fixture. The measurement parameter is displayed in Channel 2, Trace 8 "RX04_GEN2_CMRL". For Channel and Trace allocation, refer to chapter 5.2.

Observable Results:

The RX Common Mode Return Loss shall be greater than the minimum limits specified in reference [1] for 3.0G products. For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (3.0G)
150-300 MHz	5 dB
300-600 MHz	5 dB
600-1200 MHz	2 dB
1200-2400 MHz	1 dB
2400-3000 MHz	1 dB
3000-5000 MHz	1 dB

6.3.5. TEST RX-05 - Gen2(3Gb/s) Impedance Imbalance

Purpose: To verify that the Impedance Balance of the PUT receiver is within the conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.16.5

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 3.0Gb/s.   For products that support a maximum operating speed of 1.5Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

The procedure for this test is identical to that of test TX-05, with the exception that the SMA cables from port 3 and 4 of the E5071C shall be connected to the RX+ and RX- connectors of the SATA-to-SMA Test Fixture.   The measurement parameter is displayed in Channel 2, Trace 9 "RX05_GEN2_IB".   For Channel and Trace allocation, refer to chapter 5.2.

Observable Results:

The RX Impedance Balance shall be greater than the minimum limits specified in reference [1] for 3.0G products.   For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (3.0G)
150-300 MHz	30 dB
300-600 MHz	30 dB
600-1200 MHz	20 dB
1200-2400 MHz	10 dB
2400-3000 MHz	4 dB
3000-5000 MHz	4 dB (N/A for Gen2m)

6.3.6. TEST RX-06 - Gen1(1.5Gb/s) Differential Mode Return Loss

Purpose: To verify that the Differential Mode Return Loss of the PUT transmitter is within the Gen1 conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.16.6

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 1.5Gb/s. For products that support a maximum operating speed of 3.0Gb/s or 6.0Gb/s this test is not required.

Test Procedure:

The procedure for this test is identical to that of test TX-06, with the exception that the SMA cables from port 3 and 4 of the E5071C shall be connected to the RX+ and RX- connectors of the SATA-to-SMA Test Fixture. The measurement parameter is displayed in Channel 2, Trace 10 "RX06_GEN1_DMRL". For Channel and Trace allocation, refer to chapter 5.2.

Observable Results:

The RX Differential Mode Return Loss shall be greater than the minimum limits specified in reference [1] for 1.5G products. For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (1.5G)
75-150 MHz	18 dB
150-300 MHz	14 dB
300-600 MHz	10 dB
600-1200 MHz	8 dB
1200-2400 MHz	3 dB
2400-3000 MHz	1 dB

6.3.7. TEST RX-07 - Gen3(6Gb/s) Differential Mode Return Loss

Purpose: To verify that the Differential Mode Return Loss of the PUT receiver is within the Gen3 conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.16.7

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 6.0Gb/s. For products that support a maximum operating speed of 1.5Gb/s or 3.0Gb/s this test is not required.

Test Procedure:

The procedure for this test is identical to that of test TX-07, with the exception that the SMA cables from port 3 and 4 of the E5071C shall be connected to the RX+ and RX- connectors of the SATA-to-SMA Test Fixture. The measurement parameter is displayed in Channel 2, Trace 11 "RX07_GEN3_DMRL". For Channel and Trace allocation, refer to chapter 5.2.

Observable Results:

The RX Differential Mode Return Loss shall be greater than the minimum limits specified in reference [1] for 6.0G products. For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (6.0G)
300-6000 MHz	18 - 13*log10(f/300E6) dB

6.3.8. TEST RX-08 - Gen3(6Gb/s) Impedance Imbalance

Purpose: To verify that the Differential Mode Return Loss of the PUT receiver is within the Gen3 conformance limits.

References:

[1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.16.8

Last Modification: November 11, 2010 (Version 1.00RC)

Discussion:

Reference [1] provides the specifications for performing this test for the purposes of the SATA Interop Program.

This test requirement is only applicable to products that support a maximum operating speed of 6.0Gb/s. For products that support a maximum operating speed of 1.5Gb/s or 3.0Gb/s this test is not required.

Test Procedure:

The procedure for this test is identical to that of test TX-08, with the exception that the SMA cables from port 3 and 4 of the E5071C shall be connected to the RX+ and RX- connectors of the SATA-to-SMA Test Fixture. The measurement parameter is displayed in Channel 2, Trace 12 "RX08_GEN3_IB". For Channel and Trace allocation, refer to chapter 5.2.

Observable Results:

The RX Impedance Balance shall be greater than the minimum limits specified in reference [1] for 6.0G products. For convenience, the values are reproduced below.

Frequency Range	Minimum Limit (6.0G)
150-300 MHz	30 dB
300-600 MHz	30 dB
600-1200 MHz	20 dB
1200-2400 MHz	10 dB
2400-3000 MHz	10 dB
3000-5000 MHz	4 dB
5000-6500 MHz	4 dB

7. APPENDIX

Overview:

MOI appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this MOI. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this MOI. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this MOI), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

Scope:

MOI appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this MOI.

7.1.   TIME DOMAIN MEASUREMENT SETUP MANUALLY
7.1.1.   Starting Setup

1.   If TDR setup wizard appears, click **Close** button in the TDR setup wizard.

2.   Open **Setup** tab (item1).

3.   Click **Preset** (item2) under Basic to preset the E5071C.

4.   A dialog box appears requesting for confirmation. Then click **OK**.

5.   Set **DUT Topology** (item3) to **"Differential 2-Port"**.

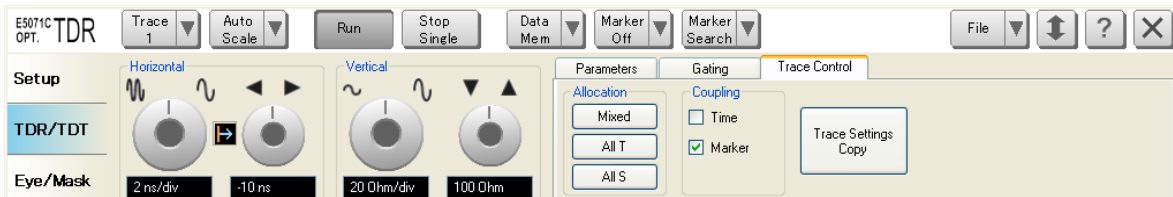6.   Click **Advanced Mode** (item4).
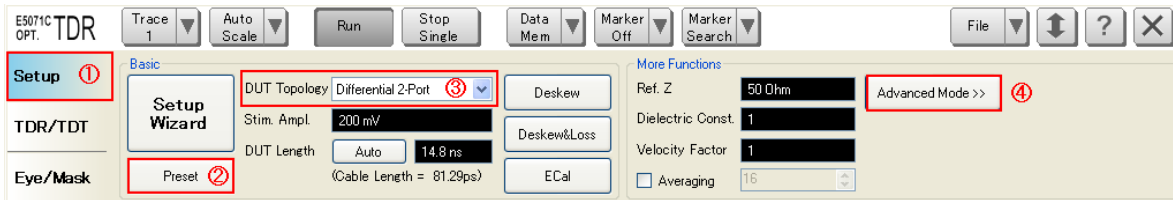
7.   A dialog box appears requesting for confirmation. Then click **Yes**. (Clear the check box for "Use Advanced Calibration Methods")
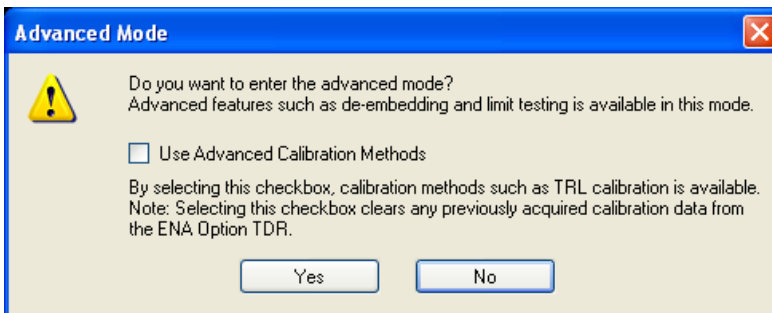
8.   Press **Display**.

9.   Click **Edit Title Label** > Enter **"Time Domain Parameters"**.

10. Click **Title Label** and turn it **ON**

11. Press **Sweep Setup** > **Power** > set **Power** to -20dBm > **Return**

7.1.2.   TX-01/RX-01 Differential Mode Return Loss

1.   Click **Stop Single**.

2.   Open **TDR/TDT** tab.

3.   Open **Trace Control** tab.

4. Clear **Time** and **Marker** check box under Coupling.

5. Select **Trace1**.

6. Open **Parameters** tab.

7. Set **Rise Time** to 100 psec (20-80%).

8. Check on **Peeling**.

9. Click the box below the left knob under Horizontal.

10. Input 1 nsec/div with the Entry dialog box.

11. Click the box below the right knob under Horizontal.

12. Input -1 nsec with the Entry dialog box.

13. Click the box below the left knob under Vertical.

14. Input 10 Ohm/div with the Entry dialog box

15. Click the box below the right knob under Vertical.

16. Input 50 Ohm with the Entry dialog box

17. Click **Maker** menu and select **1**.

18. Click **Maker Search** menu and Select **Min**.

19. Click **Maker** menu and select **2**.

20. Click **Maker Search** menu and Select **Max**.

21. Click **Maker** menu and select **3**.

22. Click **Maker** menu and select **4**.

23. Open **Trace Control** tab.

24. Click **Trace Settings Copy** button. Then Trace Settings Copy dialog box appears.

25. Select **Trace1** in the From list.

26. Select **Trace2, Trace3, and Trace5** in the To list.

27. Click **Copy**.

28. Click **Close**.

29. Select **Trace3**.

30. Open **Parameters** tab.

31. Click **Tdd22** in the parameter table.

7.1.3.   TX-02/RX-02 Single-Ended Impedance (Obsolete)

1. Select **Trace2**.

2. Open **Parameters** tab.

3. Change **Differential** to **Single-Ended**.

4. Click **T11** in the parameter table.

5. Click the box below the right knob under Vertical.

6. Input 20 Ohm with the Entry dialog box

7. Click **Maker** menu and select **2** to deactivate **Trace2**.

8. Click **Maker** menu and select **3** to deactivate **Trace3**.

9. Click **Maker** menu and select **4** to deactivate **Trace4**.

10. Press **Display** > **Equation Editor…** > Enter an equation **"T11=S11+S12"**.

11. Check **Equation Enabled** check box.

12. Click **Apply**.

13. Click **Close**.

14. Open **Trace Control** tab.

15. Click **Trace Settings Copy** button. Then Trace Settings Copy dialog box appears.

16. Select **Trace2** in the From list.

17. Select **Trace4, Trace6, and Trace8** in the To list.

18. Click **Copy**.

19. Click **Close**.

20. Select **Trace6**.

21. Open **Parameters** tab.

22. Click **T22** in the parameter table.

23. Press **Display** > **Equation Editor…** > Enter an equation **"T22=S22+S21"**.

24. Check **Equation Enabled** check box.

25. Click **Apply**.

26. Click **Close**.

27. Select **Trace4**.

28. Click **T33** in the parameter table.

29. Press **Display** > **Equation Editor…** > Enter an equation **"T33=S33+S34"**.

30. Check **Equation Enabled** check box.

31. Click **Apply**.

32. Click **Close**.

33. Select **Trace8**.

34. Click **T44** in the parameter table.

35. Press **Display** > **Equation Editor…** > Enter an equation **"T44=S44+S43"**.

36. Check **Equation Enabled** check box.

37. Click **Apply**.

38. Click **Close**.

### 7.1.4. TX-04/RX-04 Common Mode Impedance (Informative)

1. Select **Trace5**.

2. Open **Parameter** tab.

3. Select **Tcc11** in the table.

4. Click the box below the left knob under Vertical.

5. Input 5 Ohm/div with the Entry dialog box

6. Click the box below the right knob under Vertical.

7. Input 10 Ohm with the Entry dialog box

8. Click **Maker** menu and select **3** to deactivate **Trace3**.

9. Click **Maker** menu and select **4** to deactivate **Trace4**.

10. Open **Trace Control** tab.

11. Click **Trace Settings Copy** button. Then Trace Settings Copy dialog box appears.

12. Select **Trace5** in the From list.

13. Select **Trace7** in the To list.

14. Click **Copy**.

15. Click **Close**.

16. Select **Trace7**.

17. Open **Parameters** tab.

18. Click **Tcc22** in the table.

7.2. FREQUENCY DOMAIN MEASUREMENT SETUP MANUALLY
7.2.1. Channel and Trace Settings

1. Press **Display**.

2. Click **Allocate Channels** > ⊠ .

3. Press **Channel Next**.

4. Click **Num of Traces** > 12.

5. Click **Allocate Traces** > ⊞ .

6. Click **Edit Title Label** > Enter **"Frequency Domain Parameters"**.

7. Click **Title Label** and turn it **ON**

7.2.2. Common Settings

1. Press **Sweep Setup** > **Power** > set **Power** to -20dBm > **Return**

2. Click **Sweep Type** > **Lin Freq**.

3. Set **Points** to 201.

4. Press **Start** > Set start value to 300 KHz.

5. Press **Stop** > Set stop value to 8.5 GHz.

6. Press **Avg** > Set **IF Bandwidth** to 1 kHz.

7. Press **Analysis** > **Fixture Simulator** > **Fixture Simulator** and turn it **ON** > **Topology** > **Device** > **Bal-Bal** > **Return** > **BalUn ON All Traces**

7.2.3.   TX-03/RX-03 Gen2 (3Gb/s) Differential Mode Return Loss

1. Press **Trace Next** to select Trace1.
2. Press **Meas** > Select **Sdd11**.
3. Press **Scale**.
4. Set **Scale/Div** to 10 dB/div.
5. Set **Reference Value** to -40dB.
6. Press **Display** > **Equation Editor…** > Enter an equation **"TX03_Gen2_DMRL=data"**.
7. Check **Equation Enabled** check box.
8. Click **Apply**.
9. Click **Close**.
10. Press **Trace Next** to select Trace7.
11. Press **Meas** > Select **Sdd22**.
12. Press **Scale**.
13. Set **Scale/Div** to 10 dB/div.
14. Set **Reference Value** to -40dB.
15. Press **Display** > **Equation Editor…** > Enter an equation **"RX03_Gen2_DMRL=data"**.
16. Check **Equation Enabled** check box.
17. Click **Apply**.
18. Click **Close**.

7.2.4.   TX-04/RX-04 Gen2 (3Gb/s) Common Mode Return Loss

1. Press **Trace Next** to select Trace2.
2. Press **Meas** > Select **Scc11**.
3. Press **Scale**.
4. Set **Scale/Div** to 10 dB/div.
5. Set **Reference Value** to -40dB.
6. Press **Display** > **Equation Editor…** > Enter an equation **"TX04_Gen2_CMRL=data"**.
7. Check **Equation Enabled** check box.
8. Click **Apply**.
9. Click **Close**.
10. Press **Trace Next** to select Trace8.
11. Press **Meas** > Select **Scc22**.
12. Press **Scale**.
13. Set **Scale/Div** to 10 dB/div.
14. Set **Reference Value** to -40dB.
15. Press **Display** > **Equation Editor…** > Enter an equation **"RX04_Gen2_CMRL=data"**.
16. Check **Equation Enabled** check box.

17. Click **Apply**.
18. Click **Close**.

7.2.5. TX-05/RX-05 Gen2 (3Gb/s) Impedance Balance

1. Press **Trace Next** to select Trace3.
2. Press **Meas** > Select **Sdc11**.
3. Press **Scale**.
4. Set **Scale/Div** to 10 dB/div.
5. Set **Reference Value** to -40dB.
6. Press **Display** > **Equation Editor…** > Enter an equation **"TX05_Gen2_IB=data"**.
7. Check **Equation Enabled** check box.
8. Click **Apply**.
9. Click **Close**.
10. Press **Trace Next** to select Trace9.
11. Press **Meas** > Select **Sdc22**.
12. Press **Scale**.
13. Set **Scale/Div** to 10 dB/div.
14. Set **Reference Value** to -40dB.
15. Press **Display** > **Equation Editor…** > Enter an equation **"RX05_Gen2_IB=data"**.
16. Check **Equation Enabled** check box.
17. Click **Apply**.
18. Click **Close**.

7.2.6. TX-06/RX-06 Gen1 (1.5Gb/s) Differential Mode Return Loss

1. Press **Trace Next** to select Trace4.
2. Press **Meas** > Select **Sdd11**.
3. Press **Scale**.
4. Set **Scale/Div** to 10 dB/div.
5. Set **Reference Value** to -40dB.
6. Press **Display** > **Equation Editor…** > Enter an equation **"TX06_Gen1_DMRL=data"**.
7. Check **Equation Enabled** check box.
8. Click **Apply**.
9. Click **Close**.
10. Press **Trace Next** to select Trace10.
11. Press **Meas** > Select **Sdd22**.
12. Press **Scale**.
13. Set **Scale/Div** to 10 dB/div.

14. Set **Reference Value** to -40dB.

15. Press **Display** > **Equation Editor…** > Enter an equation **"RX06_Gen1_DMRL=data"**.

16. Check **Equation Enabled** check box.

17. Click **Apply**.

18. Click **Close**.

7.2.7. TX-07/RX-07 Gen3 (6Gb/s) Differential Return Loss

1. Press **Trace Next** to select Trace5.

2. Press **Meas** > Select **Sdd11**.

3. Press **Scale**.

4. Set **Scale/Div** to 10 dB/div.

5. Set **Reference Value** to -40dB.

6. Press **Display** > **Equation Editor…** > Enter an equation **"TX07_Gen3_DMRL=data"**.

7. Check **Equation Enabled** check box.

8. Click **Apply**.

9. Click **Close**.

10. Press **Trace Next** to select Trace11.

11. Press **Meas** > Select **Sdd22**.

12. Press **Scale**.

13. Set **Scale/Div** to 10 dB/div.

14. Set **Reference Value** to -40dB.

15. Press **Display** > **Equation Editor…** > Enter an equation **"RX07_Gen3_DMRL=data"**.

16. Check **Equation Enabled** check box.

17. Click **Apply**.

18. Click **Close**.

7.2.8. TX-08/RX-08 Gen3 (6Gb/s) Impedance Balance

1. Press **Trace Next** to select Trace6.

2. Press **Meas** > Select **Sdc11**.

3. Press **Scale**.

4. Set **Scale/Div** to 10 dB/div.

5. Set **Reference Value** to -40dB.

6. Press **Display** > **Equation Editor…** > Enter an equation **"TX08_Gen3_IB=data"**.

7. Check **Equation Enabled** check box.

8. Click **Apply**.

9. Click **Close**.

10. Press **Trace Next** to select Trace12.

11. Press **Meas** > Select **Sdc22**.

12. Press **Scale**.

13. Set **Scale/Div** to 10 dB/div.

14. Set **Reference Value** to -40dB.

15. Press **Display** > **Equation Editor…** > Enter an equation **"RX08_Gen3_IB=data"**.

16. Check **Equation Enabled** check box.

17. Click **Apply**.

18. Click **Close**.

7.3.   LIMIT TEST SETTINGS

7.3.1.   Displaying Judgment Result of Test

If a channel has a judgment result of fail, the fail message appears on the screen. It will be judged as failed if one or more unsatisfactory trace exists within the channel.

Follow the procedure below.

1.   Press **Analysis** > **Limit Test** > **Fail Sign** to switch the fail sign ON/OFF.

7.3.2.   Setting the Warning Beeper

Beep sound occurs when the judgment result is fail.

Follow the procedure below.

1.   Press **System** > **Misc Setup** > **Beeper** > **Beep Warning** to switch the warning beeper ON/OFF.

7.3.3.   Defining the Limit Line

Set limit lines to perform pass/fail tests.   For limit values of each measurement parameter, refer to "Observable Results" from chapter 6.2.1 to 6.2.8 and from chapter 6.3.1 to 6.3.8.

1.   Press **Channel Next** key and **Trace Next** key to activate the trace on which limit lines should be set.

2.   Press **Analysis** > **Limit Test** > **Edit Limit Line** to display the limit table shown below (Initially, no segments are entered in the limit table). Using the limit table, create/edit a segment.

	Type	Begin Stimulus	End Stimulus	Begin Response	End Response
1	MAX	0 s	600 ps	105 U	105 U
2	MIN	0 s	600 ps	75 U	75 U
3	▼				

3. Enter the limit line data following "Observable Results" from chapter 6.2.1 to 6.2.8 and from chapter 6.3.1 to 6.3.8.
4. Click **Return**.
5. Click **Limit Line** and turn it **ON**.
6. Click **Limit Test** and turn it **ON**.

7.4.   VERIFICATION OF SETUP AND CALIBRATION
    7.4.1.   Introduction

The purpose of this section is to provide a method for the verification of the overall test setup, calibration, and test fixtures prior to making measurements.

Following the setup and calibration procedure defined in chapter 5, it is desirable to perform a measurement on some pre-determined reference 'golden device', to verify that the setup and calibration are correct.

Though any known, stable device may be used as a golden device, it is convenient in this case to use a mated pair of SATA test fixtures as the reference. This provides the additional benefit of verifying the test fixtures themselves prior to making any measurements, as the fixtures are included in the measurements and are not calibrated out during the setup and calibration process. Thus, if a fixture is worn, broken, or otherwise malfunctioning, it will adversely affect the results for the PUT.

    7.4.2.   Fixture Verification

The easiest way to verify the fixtures and the test setup and calibration is simply to run the complete set of TXRX measurements on a mated pair of SATA fixtures, with the far end of the fixture pair terminated with 50 ohm loads. The results of a measurement of known good fixtures should be performed, and the results saved, to allow subsequent results to be compared for accuracy and consistency. The tests are performed using the same procedures defined for measuring a PUT, with the exception that the PUT is now a passive structure, rather than an active transceiver. Thus, the requirements for data pattern/speed, etc, do not apply.

In this section, verification measurements were performed on two pairs of fixtures (ICT and Wilder Technologies), immediately following a full calibration as specified in the procedure defined in chapter 5.3. of this MOI.   Pictures of the mated and terminated fixture pairs are shown in Figures 7-1 and 7-2.   Measurement results for the fixture pairs appear in 7.4.3. *Measurement Results*.
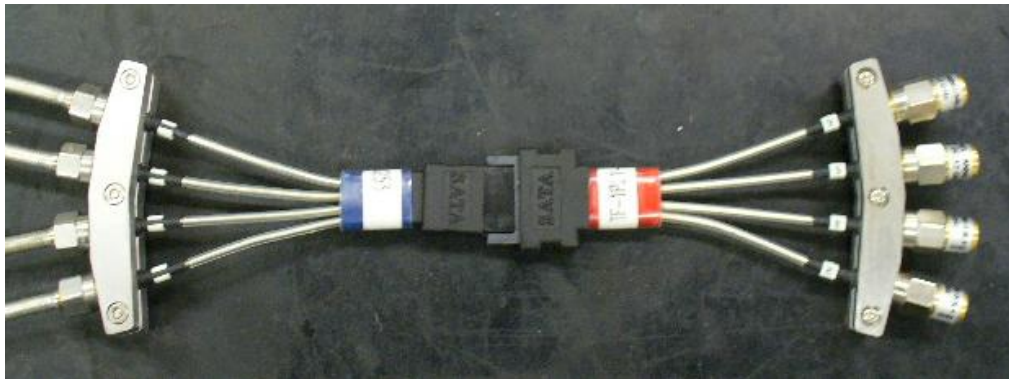
Figure 7-1: ICT Mated/Terminated Fixture Pair
**(50-ohm terminations shown on plug fixture)**

Figure 7-2: Wilder Technologies Mated/Terminated Fixture Pair
**(50-ohm terminations shown on plug fixture)**

7.4.3.   Measurement Results

Typically, one should perform all of the TXRX measurements on both signal pairs of the mated fixtures (TX and RX). Since the fixtures are symmetrical, the results should be similar for both TX and RX. For simplicity, the results for the TX pair are presented on the following pages, for both the ICT and Wilder Technologies mated pairs.
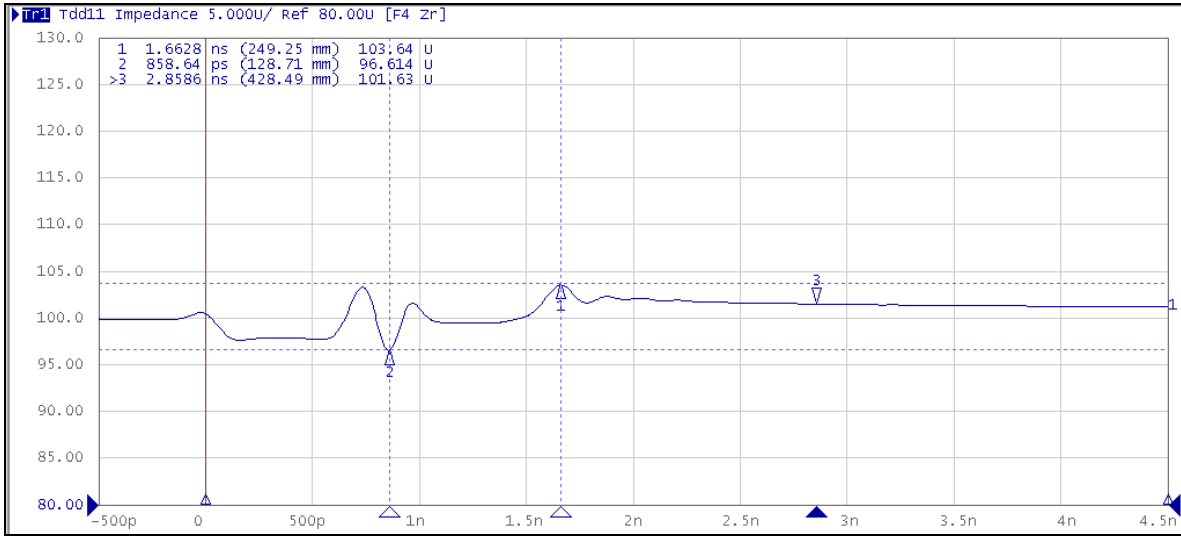
Figure 7-3: TX-01 (Diff. TDR Profile) for ICT Mated Pair
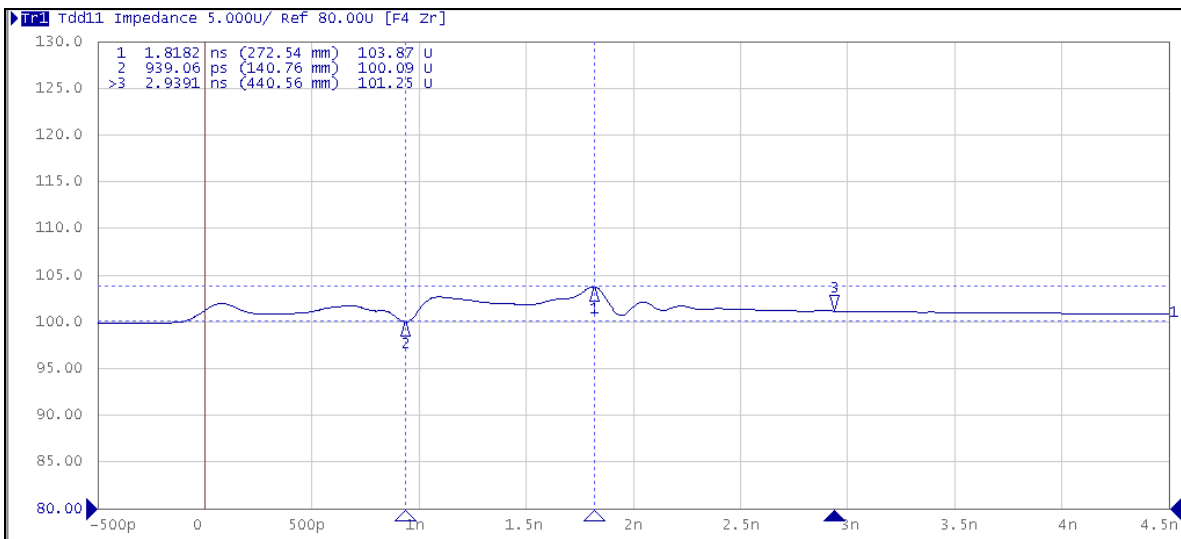
Figure 7-4: TX-01 (Diff. TDR Profile) for Wilder Technologies Mated Pair
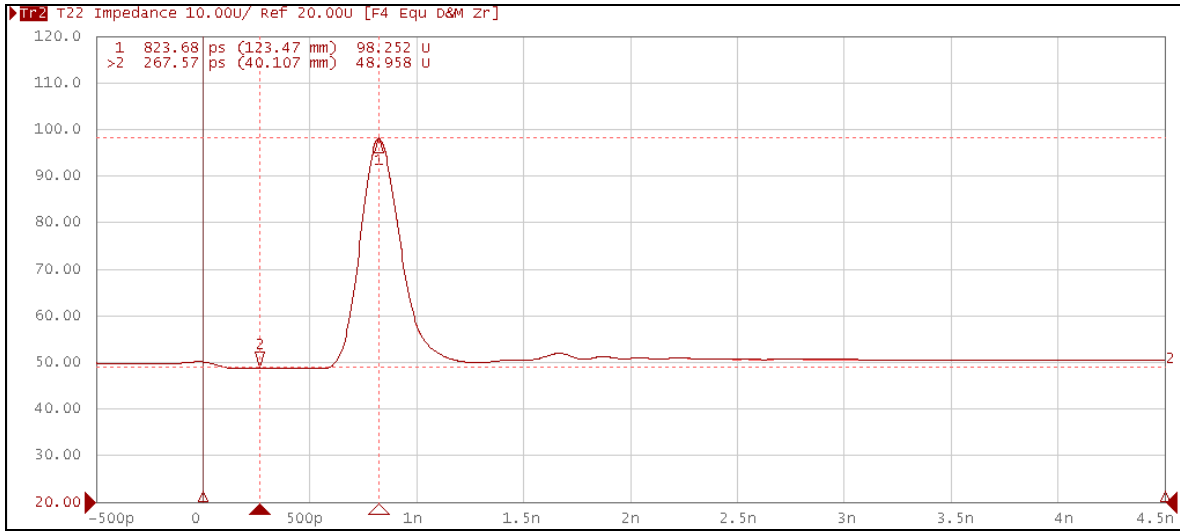
Figure 7-5: TX-02 (Single-Ended Impedance) for ICT Mated Pair
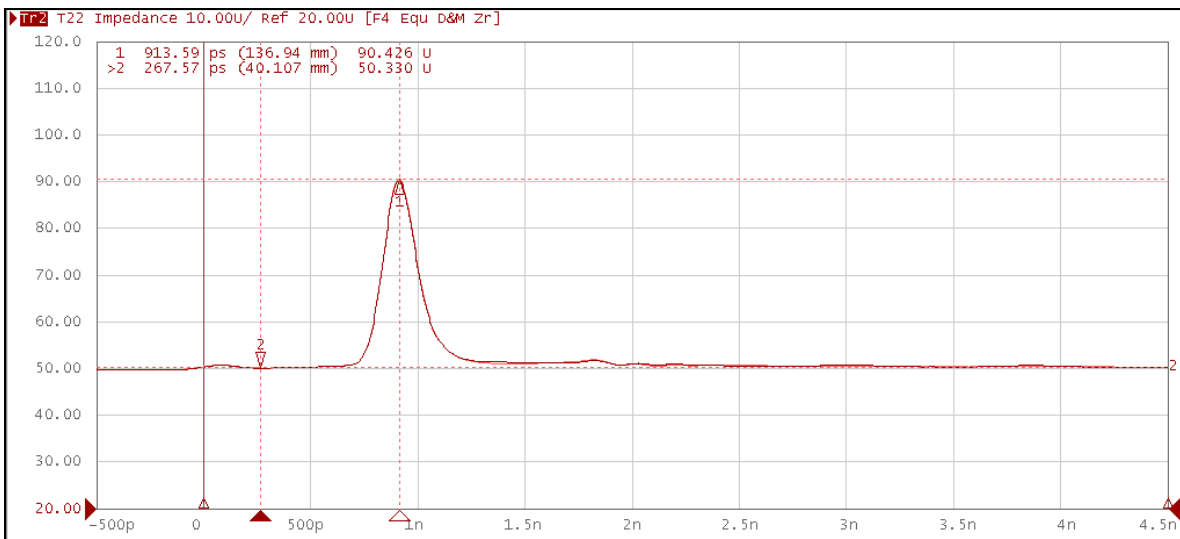
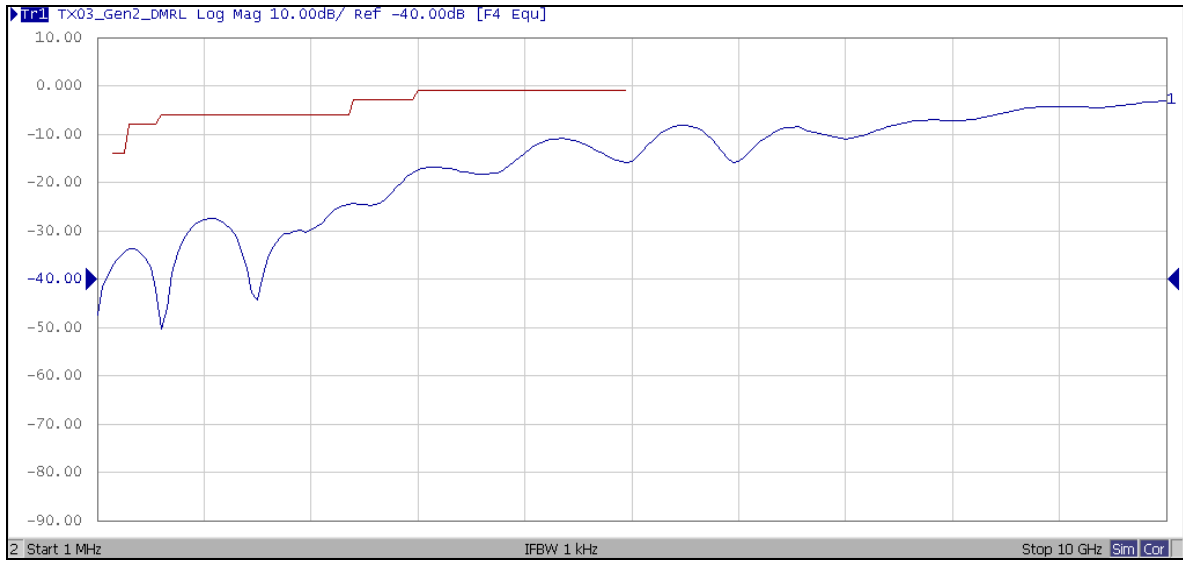**Figure 7-6: TX-02 (Single-Ended Impedance) for Wilder Technologies Mated Pair**

Figure 7-7: TX-03 (Diff. Return Loss) for ICT Mated Pair

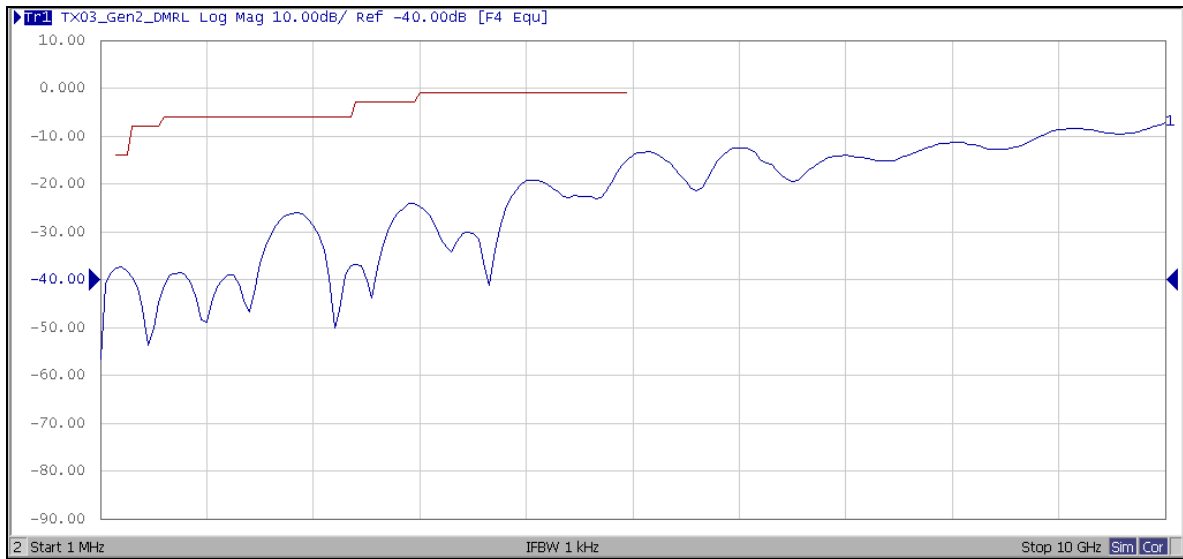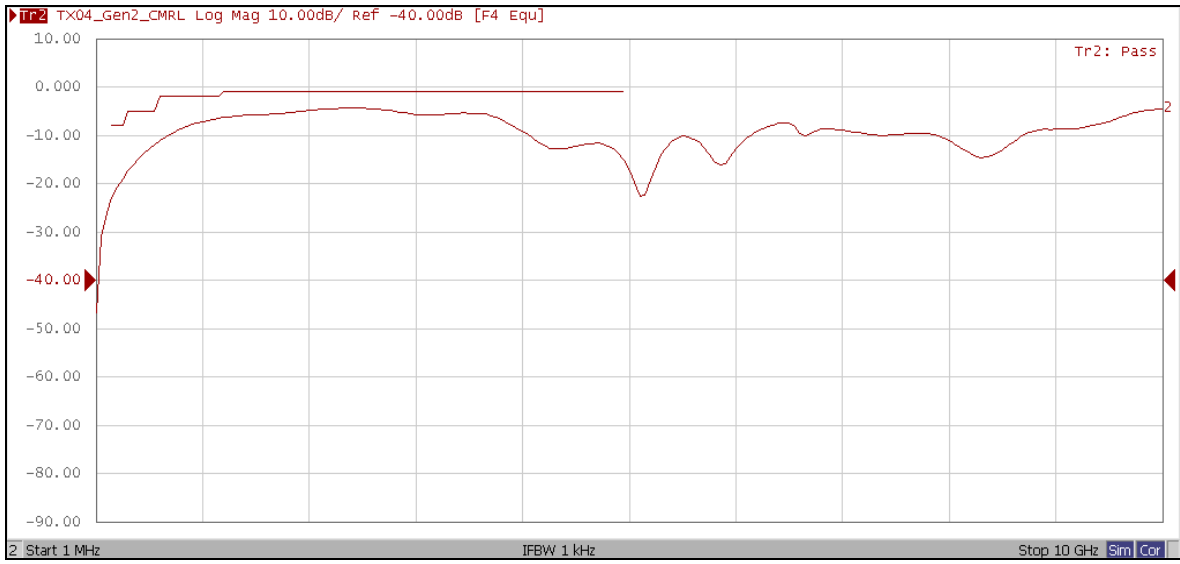**Figure 7-8: TX-03 (Diff. Return Loss) for Wilder Technologies Mated Pair**
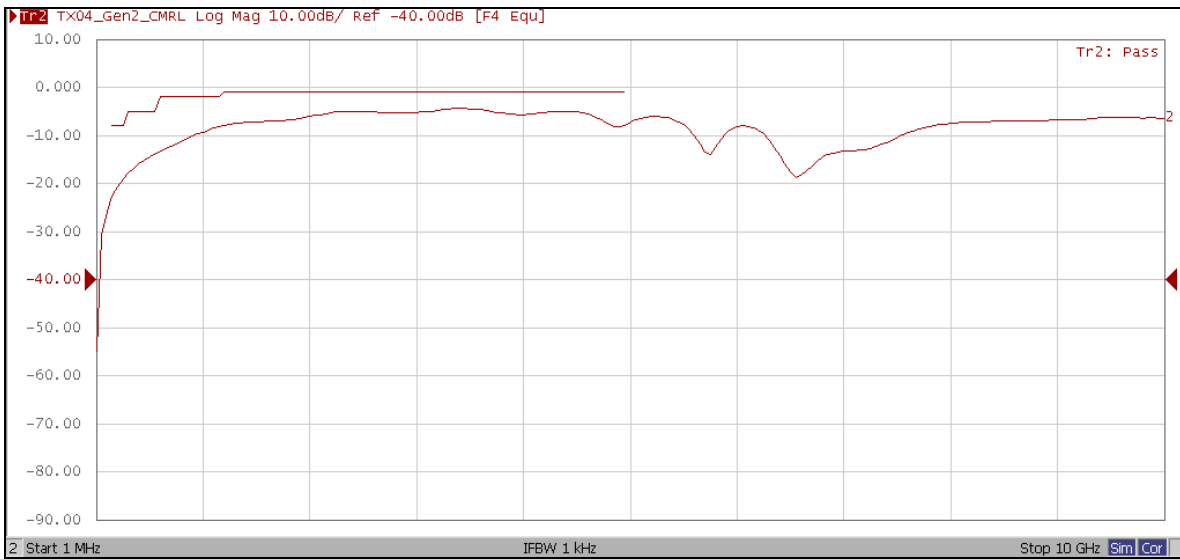
Figure 7-9: TX-04 (Common-Mode Return Loss) for ICT Mated Pair

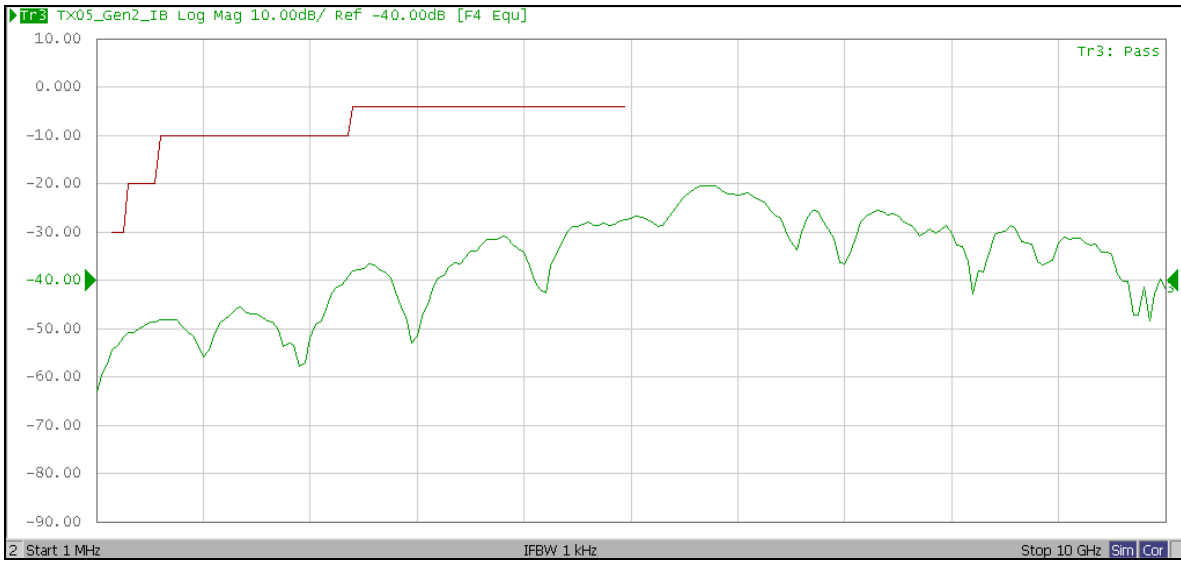**Figure 7-10: TX-04 (Common-Mode Return Loss) for Wilder Technologies Mated Pair**
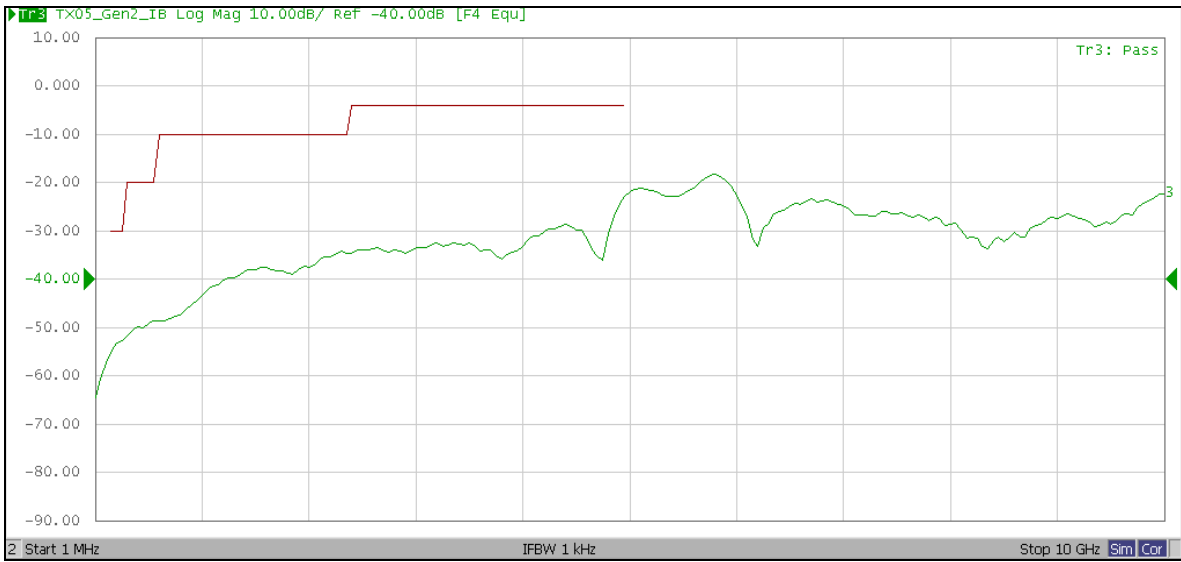
Figure 7-11: TX-05 (Impedance Imbalance) for ICT Mated Pair

Figure 7-12: TX-05 (Impedance Imbalance) for Wilder Technologies Mated Pair

7.4.4. Summary

In this appendix, a method was described which would allow for the simultaneous verification of the test setup and calibration, as well as the test fixtures used for the tests. The method consists simply of using the mated pair of test fixtures as a 'golden' reference device, which are measured post-calibration, and prior to performing the actual PUT measurements, to ensure that the setup, calibration, and test fixtures are all valid.

Sample result data was presented for the TX pair of the mated fixture pair for two commonly available fixtures from ICT and Wilder Technologies. These show typical performance results, and are provided for informative purposes, showing they typical margin expected from these types of fixtures. It should be noted that fixtures from different vendors (and even different samples from the same vendor) may have slightly different performance margin. The amount of margin should be considered when evaluating fixtures, as the more margin the fixtures have, the better the overall measurement will be.